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EP 0191201 A1 EP 0163203 A2 EP 0064829 A2

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(54) Ohmic contacts for semiconductor devices

(57) In a method for forming a shallow ohmic contact to a buried layer 3 of a semiconductor device, an opening is etched down to the interface 11 of the heterostructure 3, 5 and is overlaid with a contact material 33 which is diffused 37 into the structure to make contact with a 2-dimensional electron gas 15. The diffusion takes place during annealing and the device may be a HEMT.

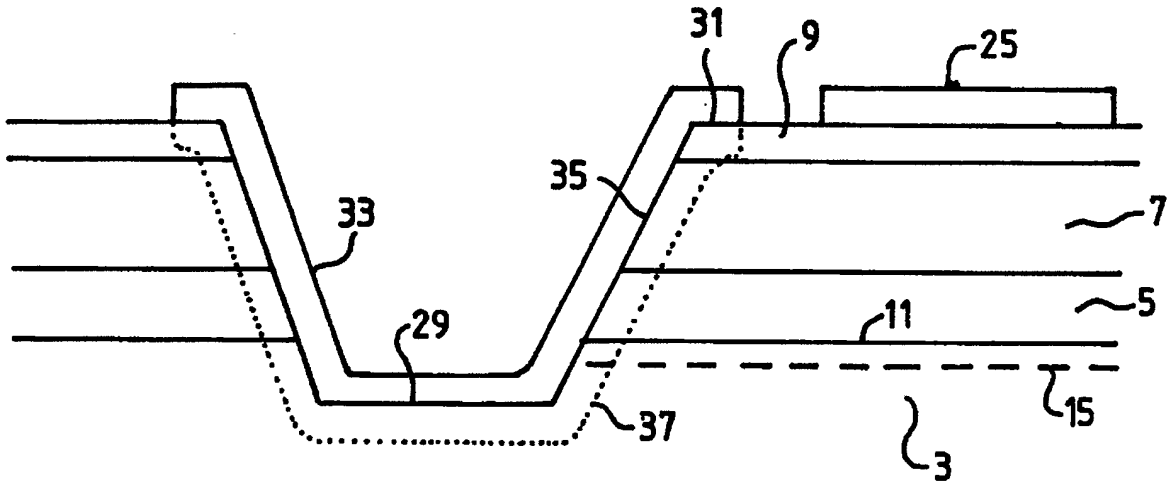

FIG. 5

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

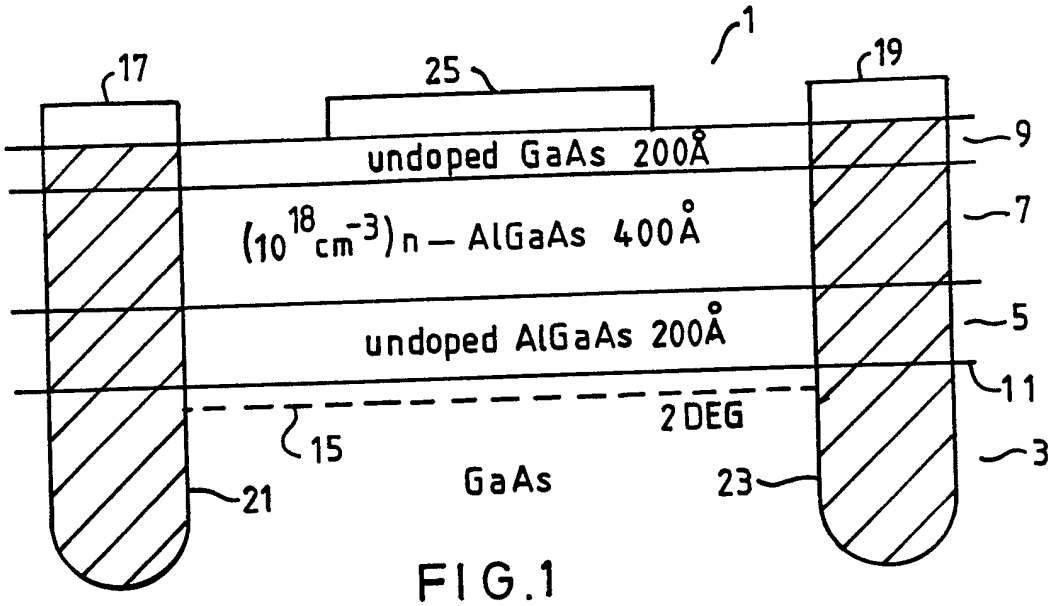

FIG.1

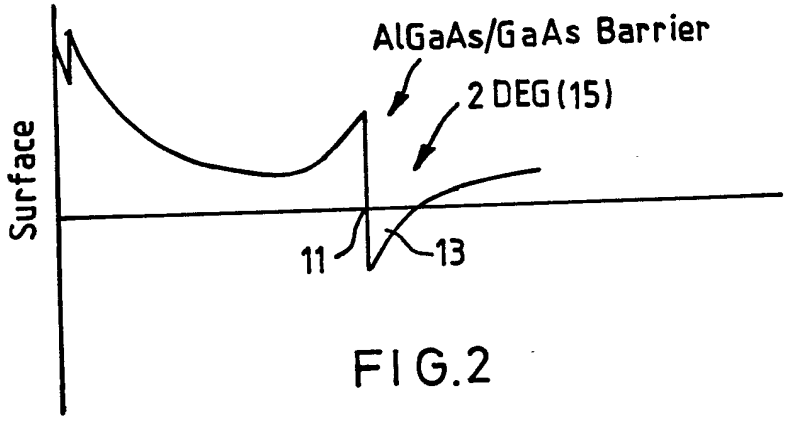

FIG.2

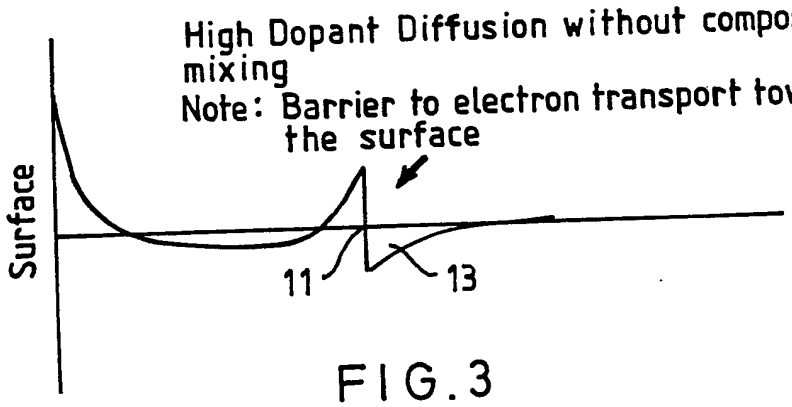

FIG.3

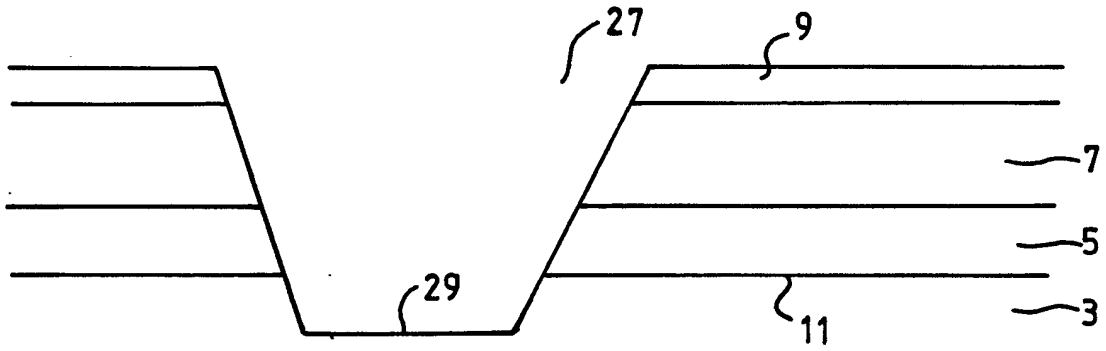

FIG. 4

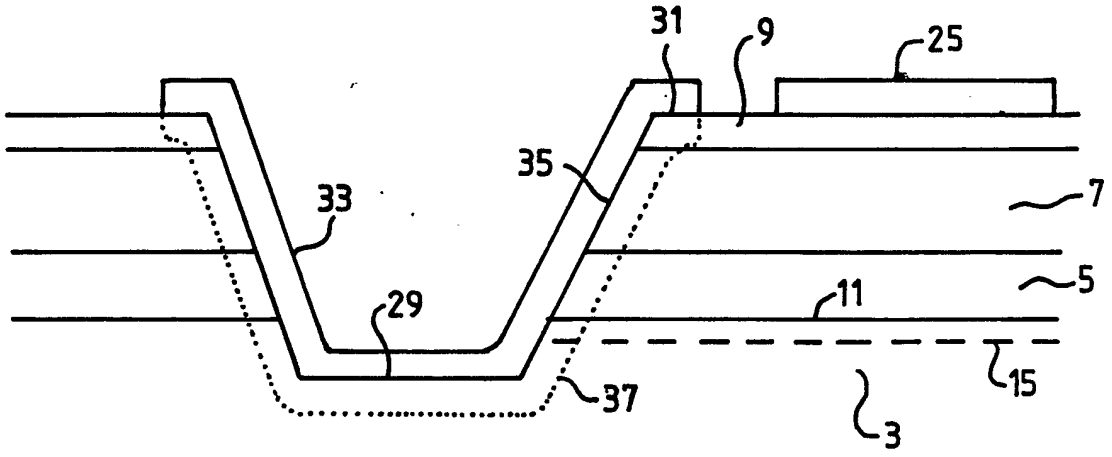

FIG. 5

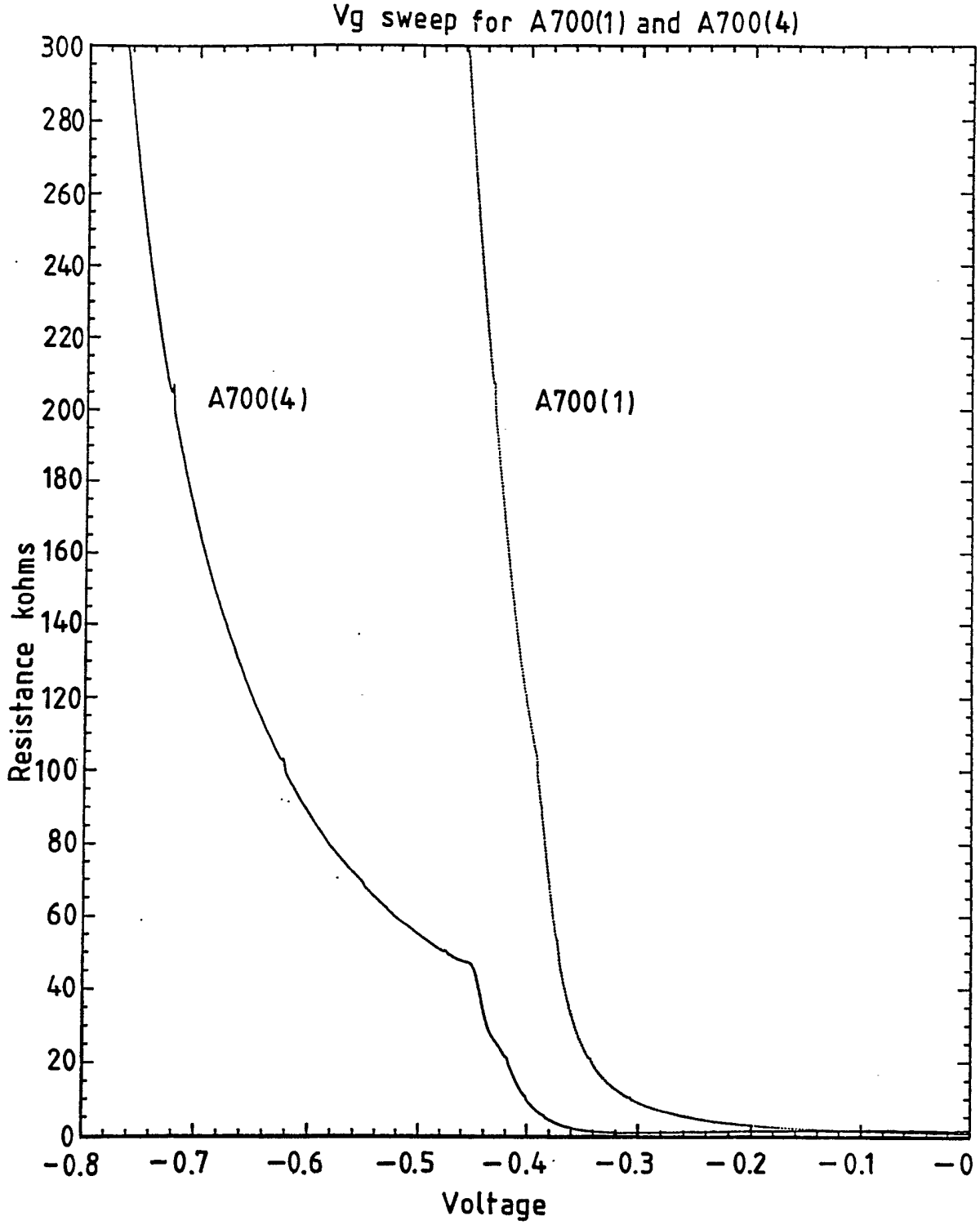
Vg sweep for A700(1) and A700(4)
A700(4)
A700(1)
Resistance kohms
Voltage
300
280
260
240
220
200
180
160
140
120
100
80
60
40
20
0
-0.8
-0.7
-0.6
-0.5
-0.4
-0.3
-0.2
-0.1
-0

FIG.6

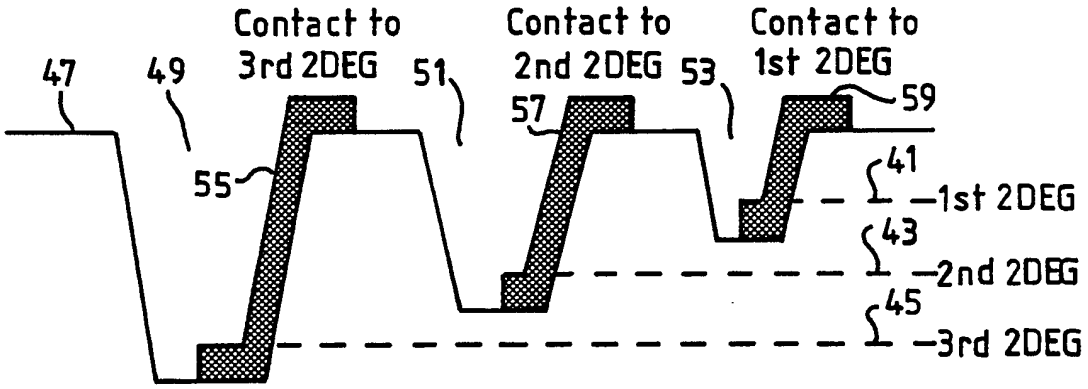
Contact to
3rd 2DEG
Contact to
2nd 2DEG
Contact to
1st 2DEG
47
49
51
53
55
57
59
41
1st 2DEG
43
2nd 2DEG
45
3rd 2DEG

FIG.7

SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME

The present invention is concerned with a method of making an ohmic contact to a heterojunction-type semiconductor device and the device resulting from such method.

A typical heterojunction device is a high electron mobility effect transistor (HEMT). This uses a heterostructure such as GaAs/AlGaAs to create a so-called two dimensional electron gas (2DEG), in which the wavefunction perpendicular to the layers is quantised in energy and electrons are confined in the GaAs layer near the GaAs/AlGaAs hetero-interface but can move freely in a plane close and parallel to the interface.

By separating donor impurities from the electron conducting channel, ie., by doping the AlGaAs layer, the 2DEG may exhibit very high mobilities (of the order of 10^6 cm^2/Vs). This is utilized in HEMTs, MODFETs (Modulation Doped Field Effect Transistors) and the like. The HEMT finds application in such areas as microwave amplifiers and high speed integrated circuits.

In ordinary field effect transistors, conductivity modulation ΔG is effected through the change of carrier density ΔN within a channel. This sets a speed limit of about 1 picosecond using high-velocity electrons ($\simeq 2 \times 10^7$ cm/s) travelling over a channel distance of 0.2 μm.

Figure 1 of the accompanying drawings shows a typical HEMT structure 1. This comprises an undoped GaAs active layer 3 above which, in order, are an undoped AlGaAs spacer layer 5 (e.g. 200Å thickness), an n-doped

AlGaAs barrier layer 7 (e.g. with impurity concentration around 10^{18} cm^{-3}, 400Å thickness) and a cap layer 9 (e.g. 100Å thickness).

Figure 2 shows the energy band diagram of the HEMT according to Figure 1. Electrons are transferred to the AlGaAs/GaAs interface 11 from the doped barrier layer 7 and form a channel 13 in the active layer, adjacent to the interface in which the 2DEG 15 is confined.

However, carriers are free to move perpendicular to the layers so that a current can flow between a source 17 and drain 19, spaced apart and contacting the 2DEG in the buried active layer (see Figure 1) as respective ohmic contact regions 21,23.

A gate electrode 25 above the cap layer switches the current flowing between source and drain, by affecting the number of carriers. Electrons are able to occupy sub-bands in the potential well of the channel but if the carrier density is sufficiently small, only the ground-state is occupied. The Schottky barrier formed at the surface changes the carrier density.

Unfortunately, the abrupt energy level change at the interface, necessary for forming the potential well to contain the 2DEG, creates a significant problem for forming ohmic contacts for the source and drain.

Due to the high concentration of localised states at the GaAs surface, the Fermi level under all conditions except UHV cleaving of the (110) facet is pinned near the centre of the bandgap. This results in the depletion of charge carriers near the surface in doped samples, with the depletion width depending on the inverse square root of the bulk material doping

concentration. The high surface state density also results in an almost work-function independent Schottky barrier height between GaAs and all metals. Thus a metal contact made to n-doped GaAs will result in a non-ohmic contact (non-linear current versus voltage behaviour), even if the work-function of the metal is of the order of the electron affinity.

Conventionally, the two main techniques to form an ohmic contact with a GaAs layer are either to diffuse dopant in underneath the contact or to form another material phase between the contact and the GaAs which results in Fermi level pinning near the conduction band. By diffusing a high concentration of dopant such as Ge into the surface region under the contact the depletion depth is reduced to such an extent that tunnelling through the barrier becomes the dominant transport mechanism. This gives ohmic behaviour over the current range of interest. There are many contact technologies that work using this effect such as GePd, GeAg and NiGeAu etc.

However, the formation of an ohmic contact to a HEMT structure is more complicated because of the buried abrupt junction (e.g. AlGaAs/GaAs) inherent in this structure. This barrier, especially at low temperatures is very effective in inhibiting current flow between the contact and the 2DEG even if the above condition is met.

Figure 3 is an energy diagram showing the effect of merely carrying out a conventional high dopant diffusion to a HEMT structure as shown in Fig. 1 to form the ohmic contacts 21,23. Whilst the effect of the Schottky barrier arising at the metal contact is greatly mitigated, the GaAs/AlGaAs interface still present a high and sharp barrier to conduction.
Moreover, in order to achieve ohmic contact to the

heterostructure using the conventional methods, one either has to use a higher than normal diffusion temperature or else a higher than usual concentration of diffused dopant, so that the buried interface is "blurred". This results in a deep contact which for some devices, prevents them from functioning as intended.

One such device is a so-called velocity modulation transistor (VMT). A VMT is a derivative of the conventional HEMT. Switching of the source-to-drain current is achieved not by changing the number of carriers but by affecting their mobilities. A VMT typically has a pair of barrier layers sandwiching the active layer, with a respective gate electrode on either side. These are normally referred to as the front gate (on top of the structure) and the back gate (on the substrate side).

Using the conventional method, with (say) GeAu contacts, results in a leaky back gate. This makes it important to prevent diffusion of the dopant beyond the inverted hetero-interface.

We have now found a method of forming a shallow ohmic contact which overcomes this problem. Thus, the present invention provides a method of forming a shallow ohmic contact to a buried layer of a heterojunction semiconductor device in which said buried layer is part of a heterostructure and forms an interface with an adjacent layer of the heterostructure such that the interface presents an abrupt energy barrier, the method comprising the steps of:-

(i)etching a region of the heterostructure to expose the buried layer;

(ii)applying a contact material to the etched region to contact the buried layer; and

(iii)annealing the device to form an ohmic contact between the contact material and the buried layer.

The present invention also provides a heterojunction semiconductor device comprising a buried layer and an adjacent layer of a heterostructure defining an interface therebetween, an opening being provided in said heterostructure down to said buried layer, and a contact material overlying the opening and forming an ohmic contact with said buried layer.

The present invention is especially useful for forming ohmic contacts in HEMT or VMT structures. In terms of a HEMT or VMT structure, a "shallow" ohmic contact means one extending down to but not substantially beyond the active layer of interest, ie, down to the 2DEG.

The present invention allows very shallow ohmic contacts to be formed and has been demonstrated to be capable of making contact to a 2DEG without contacting another layer which is separated by only a 200Å AlGaAs barrier.

The contact materials used can be any materials usable to make conventional ohmic contacts with GaAs and other semiconductor materials. For devices intended to operate at low temperatures, GePd is greatly preferred, although this is not a requirement, the usual combinations may be used for example NiInW, GeInW, GePd, NiGeAs, GeAg, etc..

As is well known, when for example GePd is used to make an ohmic contact with (say) n^+- GaAs, excess Ge is used as a layer on top of a Pd layer. On annealing, these two elements intermix and excess Ge diffuses into the wafer to displace Ga from some crystal sites. First, some of the Ga reacts with Pd leaving vacant

crystal sites, then Ge reacts with Pd. Finally, the excess Ge diffuses into the crystal structure and occupies the vacant Ga sites.

GePd is especially useful as the contact material for the present invention because this diffusion will occur at relatively low temperatures with GaAs, for example from 300 to 400^{o}C. With the present invention, the Ge or analogous material can diffuse into the structure/sides of the opening to a depth of up to (say) from 50Å to 250Å, typically around 100Å to form the ohmic contact.

It is advantageous, although not absolutely necessary, for the etched opening to extend below the interface. Typically, it may extend from 50Å to 250Å, e.g. around 100Å below. The minimum etch depth is set by the tunneling distance which typically is about 100Å shallower than the 2DEG. The maximum depth for practical purposes is about double the distance of the 2DEG.

To make selective ohmic contacts to a plurality of buried layers at different depths, e.g. to manufacture stacked devices, a plurality of openings may be etched to different depths, each with its own respective contact layer.

In general, the present invention is applicable not only to AlGaAs/GaAs systems but to any structure where there is a large band discontinuity, for example InGaAs/AlInAs or InGaAs/InP.

The present invention will now be explained in more detail by the following description of a preferred embodiment and with reference to the accompanying

drawings in which:

Figure 1 shows a typical HEMT structure with conventional ohmic contacts;

Figure 2 is an energy diagram for the HEMT structure shown in Figure 1;

Figure 3 shows the effect on the energy diagram of a conventional diffusion process for making an ohmic contact to the 2DEG in the structure shown in Figure 1;

Figure 4 shows a first stage in carrying out a method according to the present invention;

Figure 5 shows a second stage of a method according to the present invention;

Figure 6 is a voltage versus resistance plot demonstrating selective ohmic contact to one or two 2DEGs; and

Figure 7 shows a further embodiment for effecting selective shallow ohmic contact to a plurality of buried layers at different depths.

Figure 4 shows a first stage of forming a shallow ohmic contact in accordance with the present invention. In Figures 4 and 5, reference numerals in common with Figure 1 denote the same features.

A heterostructure comprising the GaAs active layer 3, AlGaAs spacer layer 5, n-AlGaAs barrier layer 7 and GaAs cap layer 9 is grown in the normal way. Then, using a mask (not shown) to effect selective etching, a via 27 is etched into the structure. The bottom 29 of the via is about 100Å below the interface 11.

Then, a Pd layer followed by a Ge layer in excess to the Pd are applied over the inside of the via, typically with a ratio of Ge:Pd of 1:1.5 and with a thickness of about 500Å. This layer overlaps the unetched rim 31

of the cap layer and is annealed at about 350°C to form an ohmic contact layer 33 as shown in Figure 5. This contact layer extends from the rim 31 to the bottom 29 of the via 27.

During the annealing process, the Ge diffuses through the bottom 29 and side walls 35 of the via to an extent of about 100Å as denoted by the dotted line 37. Numeral 15 shows where the 2DEG would be during operation of the device, at a depth of about 10Å from the interface 11. It can be seen that the diffused Ge is at the same depth as the 2DEG to make the ohmic contact therewith.

The gate electrode 25 can be applied subsequent to formation of the ohmic contact.

To demonstrate the feasibility of making selective contact to only one 2DEG or two 2DEG's at adjacent interfaces, the resistance versus applied gate voltage was measured for a HEMT structure of the general kind shown in Figure 1. In this device, the first 2DEG was 700Å below the upper surface of the structure and the second 2DEG was 400Å below the first.

The results are shown in Figure 6. The curve labelled A700(1) was obtained using a device where the via was etched to a depth about 100Å above the first 2DEG. The curve A700(4) is for an equivalent device in which the via was etched to a depth approximately equal to that of the second 2DEG. The discontinuity in the latter curve is indicative of ohmic contact being made to the second (lower) 2DEG.

The via can thus be etched to an appropriate depth to enable contact to a 2DEG of interest. This means that a

plurality of 2DEGs at different depths can be selectively contacted by means of a series of vias etched to different depths. An example of such an arrangement is shown in Figure 7.

First, second and third 2DEGs are, in that order, formed in progressivly deeper buried layers and are denoted, respectively, by reference numerals 41, 43, 45, below the surface 47. To contact these, three vias 49, 51, 53 are etched to appropriate depths. Via 49 is the deepest and via 53 is the most shallow, with via 51 having a depth between the latter two.

Each via 49, 51, 53 is provided with a respective ohmic contact layer 55, 57, 59 extending to the bottom of each via in the same manner as the contact layer 33 is formed in the embodiment shown in Figures 4 and 5. The three ohmic contact layers 53, 57, 59 in the present embodiment respectively contact the first, second and third 2DEGs denoted by numerals 41, 43, 45 by virtue of the depths of the different vias.

Such a system can be applied to making selective contact to two or more buried layers and makes possible the vertical stacking of devices. The etching in such an arrangement fulfils two purposes as the unmetallised portion also serves to deplete the conducting layer, ensuring that adjacent layers are not shorted together by the ohmic contact.

In the light of this disclosure, modifications of the described embodiment as well as other embodiments, all within the scope of the appended claims will now become apparent to persons skilled in the art.

CLAIMS

1. A method of forming a shallow ohmic contact to a buried layer of a heterojunction semiconductor device in which said buried layer is part of a heterostructure and forms an interface with an adjacent layer of the heterostructure such that the interface presents an abrupt energy barrier, the method comprising the steps of: -

(i)etching a region of the heterostructure to expose the buried layer;

(ii)applying a contact material to contact the buried layer; and

(iii)annealing the device to form an ohmic contact with the buried layer.

2. A method according to claim 1, wherein the etching step is effected to etch the buried layer beyond the interface.

3. A method according to claim 1 or claim 2, wherein the buried layer comprises GaAs and forms the interface with an adjacent AlGaAs layer.

4. A method according to any preceding claim, wherein the contact material is GePd.

5. A method according to any preceding claim, wherein the heterostructure is a HEMT structure.

6. A method according to any preceding claim, wherein a plurality of regions are etched to different depths in step (i) to allow formation of ohmic contacts selectively contacting a plurality of buried layers at different depths.

7. A heterojunction semiconductor device comprising a buried layer and an adjacent layer of a heterostructure defining an interface therebetween, an opening being provided in said heterostructure down to said buried layer and a contact material overlying the opening and forming an ohmic contact with said buried layer.

8. A device according to claim 7, wherein the opening extends to below the interface.

9. A device according to claim 7 or claim 8, wherein said opening extends below the interface.

10. A device according to any of claims 7 to 9, wherein the buried layer comprises GaAs and forms the interface with an adjacent AlGaAs layer.

11. A device according to any of claims 7 to 10, wherein the contact material is GePd.

12. A device according to any of claims 7 to 11, wherein the heterostructure is a HEMT structure.

13. A device according to any of claims 7 to 12, comprising a plurality of openings of different depths permitting selective ohmic contact to a plurality of buried layers at different depths.

14. A method of forming a shallow ohmic contact to a buried layer of a heterojunction semiconductor device, the method being substantially as hereinbefore described with reference to Figures 4, 5 and 7 of the accompanying drawings.

15. A heterojunction semiconductor device substantially as hereinbefore defined with reference to Figure 5 or Figure 7 of the accompanying drawings.

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Examiner's report to the Comptroller under Section 17 -12-
(The Search report)

Application number
GB 9313876.6

Relevant Technical Fields

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(ii) Int Cl (Ed.5) H01L

Search Examiner
C D STONE

Date of completion of Search
21 OCTOBER 1993

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE DATABASES : WPI

Documents considered relevant following a search in respect of Claims :-
ALL

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	EP 0191201 A1	(PHILIPS) - see Figure 3	1, 7
X	EP 0163203 A2	(TEXAS) - see Figure 3	1, 7
X	EP 0064829 A2	(FUJITSU)	1, 7

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